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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/516,004	02/29/2000	Isik C. Kizilyalli	46-19-123	9672

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EXAMINER

NADAV, ORI

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 12/28/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/516,004

Applicant(s)

KIZILYALLI ET AL.

Examiner

ori nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 16 October 2001.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) 1-5 and 12-23 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                             | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other:  |

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## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 6-8 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification recites the initial formation of self-aligned source and drain regions. The drawings illustrate that subsequent processing steps result in a final structure whose source and drain regions are not self-aligned with the gate electrode. Thus, there is no support for operable self-aligned FET, as recited in claim 6.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

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4. Claims 6-7, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(e) as being anticipated by Yu (6,194,748).

Yu teaches in figure 1 an integrated circuit comprising a semiconductor material 14 of the first conductivity type, a FET gate structure on the semiconductor material comprising a conductive layer 36 and an amorphous tantalum pentoxide 34 (column 5, lines 50-55) formed between the conductive layer and the semiconductor material and having a dielectric constant greater than 5, source and drain regions 17, 19 of the second conductivity type along the surface region of the semiconductor material configured to form an operable FET, and being directly with the gate structure.

Although Yu does not teach source and drain regions being formed self-aligned with the gate structure, forming source and drain regions self-aligned with the gate structure are processing limitations which do not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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6. Claims 6-7 and 9-11, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (6,194,748) in view of Admitted Prior Art (APA) or Shinriki et al. (5,292,673).

Yu teaches in figure 1 an integrated circuit comprising a semiconductor material 14 of the first conductivity type, a FET gate structure on the semiconductor material comprising a conductive layer 36 and an amorphous tantalum pentoxide 34 (column 5, lines 50-55) formed between the conductive layer and the semiconductor material and having a dielectric constant greater than 5, source and drain regions 17, 19 of the second conductivity type along the surface region of the semiconductor material configured to form an operable FET, and being directly with the gate structure.

Yu does not teach in the embodiment of figure 1 self-aligned source and drain regions.

Yu teaches forming source and drain regions self-aligned with the gate structure (column 1, lines 6-27). APA teaches that it is conventional to form self-aligned source and drain regions (page 7, lines 3-9). Shinriki et al. teach in figure 6a self-aligned source and drain regions 11 (column 5, lines 30-31).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the source and drain regions being self-aligned with the gate structure in Yu's device, because it is conventional in the art to form self-aligned source and drain regions in order to simplify the processing steps, of which judicial notice is taken.

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Regarding claims 9-11, the claimed limitations of a gate leakage current being less than one milliamp per cm<sup>(-2)</sup> during operation are inherent in Yu's device, because Yu's structure is identical to the claimed structure.

7. Claim 8, insofar as in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu, APA and Shinriki et al., as applied to claim 6 above, and further in view of Endo (5,596,214).

Yu, APA and Shinriki et al. teach substantially the entire claimed structure, as applied to claim 6 above, except a layer of silicon oxide disposed between the insulative layer and the surface region.

Endo teaches in figure 3a layer of silicon oxide disposed between the insulative layer and the surface region (column 14, lines 57-58). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a layer of silicon oxide disposed between the insulative layer and the surface region in prior art's device in order to improve the leakage current characteristics of the device.

### ***Response to Arguments***

8. Applicant argues on page 5 that Yu does not teach source and drain regions being formed directly self-aligned with the gate structure, because Yu teaches source and drain extension regions.

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The phrase source and drain regions being formed directly self-aligned with the gate structure does not mean that the source and drain regions can not have "source and drain extension regions'. The source and drain extension regions are part of the source and drain regions. Furthermore, the term "directly" does not mean that the device does not include an LDD region and it does not mean that the heavily doped source and drain regions are self-aligned with the gate structure.

9. Applicant argues on pages 3-6 that the selective annealing process of the present invention results in advantages which are not achievable in conventional prior art.

Applicant did not specify which structural elements are produced as a result of the selective annealing process of the present invention which are not present in the device of Yu, APA, Shinriki et al. and Endo.

10. The rest of applicant's arguments with respect to claims 6-11 have been considered but are moot in view of the new ground(s) of rejection.

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***Conclusion***

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

**Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722**

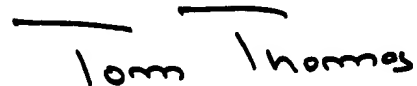


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and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772**.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**



TOM THOMAS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800

Ori Nadav

December 20, 2001